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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,918	09/22/2003	Masanori Ogura	03500.017569.	5148
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FITZPATRICK CELLA HARPER & SCINTO 30 ROCKEFELLER PLAZA NEW YORK, NY 10112			EXAMINER	
			KHAN, USMAN A	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/664,918	Applicant(s) OGURA ET AL.
	Examiner USMAN KHAN	Art Unit 2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 28 February 2008.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-3 and 5-16 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-3 and 5-16 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 22 September 2003 and 08 March 2007 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date 9/22/2003

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

Applicant is advised that the Notice of Allowance mailed on 2/15/2008 is vacated. If the issue fee has already been paid, applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may wait until the application is either found allowable or held abandoned. If allowed, upon receipt of a new Notice of Allowance, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a specified Deposit Account.

The indicated allowability of claims 1-3 and 5 - 16 is withdrawn in view of the newly discovered reference(s) to Applicants admitted Prior Art in further view of YAMAMURA et al. Rejections based on the newly cited reference(s) follow.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 2/28/2008 (Which was originally filed on 9/22/2003 but was not in the USPTO system at the time of examination) has now been considered by the examiner. The submission is in compliance with the provisions of 37 CFR 1.97.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 - 2 and 5 - 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (hereafter referred as AAPA; note the examiner is using the PgPub 2004/0057719 to refer to the paragraph numbers and such) in view of YAMAMURA et al. (US PgPub 2002/0025164).

Regarding **claim 1**, AAPA teaches a solid state image pick-up device formed on a chip, comprising: a pixel region; a first shift register for reading a signal charge from the pixel region (figure 8, item 205; Note: figures 7A,7B and 8 are prior art and the applicant has submitted an amendment to the drawing to label these figures as prior art); a second shift register having a lower driving frequency than that of the first shift register (figure 8, item 202 and paragraph 0014), wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8, items 205 and 202); an amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 8 item 207), outputting video signals (note this outputting of the video signal is not associated with any component as claimed so the examiner can consider any item such as item 207, 201, 204, 206 or any component as outputting video signal to be used later, in this case the examiner chooses item any one or a combination of these items).

However, AAPA fails to disclose a pad for outputting the video signals to an outside of the chip, the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged.

YAMAMURA et al., on the other hand teaches a pad for outputting the video signals to an outside of the chip, the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged.

More specifically, YAMAMURA et al. teaches a pad for outputting the video signals to an outside of the chip, the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged (figures 1 – 2; pads arranged along vertical side of the chip away from the horizontal side when the horizontal registers are located).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of YAMAMURA et al. with the teachings of AAPA because in page 1 lines 5 – 8 and page 5 lines 4 – 17 also paragraphs 0009, 0012, 0013, and 0016 YAMAMURA et al. teaches that using the invention flaring problems can be reduced and corrected which in turn will produce an improved image.

Regarding **claim 2**, as mentioned above in the discussion of claim 1, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that wherein in the pixel region, pixels having an active element are two-dimensionally arranged (figure 7A and 8 with active elements 201, 204, and 206).

Regarding **claim 5**, as mentioned above in the discussion of claim 2, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that the pixel region is formed into a rectangle, and the first shift register is arranged closer to a long side of the pixel region (figure 7A and 8 with first shift register 205 in figure 8 in the horizontal location).

Regarding **claim 6**, as mentioned above in the discussion of claim 5, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that the pixel region is sandwiched by shift registers (figure 8 items 202 and 205 sandwiching the pixel region).

Regarding **claim 7**, as mentioned above in the discussion of claim 2, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that the first shift register is a horizontal shift register, and the second shift register is a vertical shift register (figure 8 items 202 vertical shift register and 205 horizontal shift register).

Regarding **claim 8**, as mentioned above in the discussion of claim 1, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim.

Additionally, AAPA teaches a signal processing unit for processing a signal from the solid state image pick-up device (Paragraphs 0005 – 0018,

processing of the pixels and outputting of the image is done by a processor even though it is not specifically discussed).

However, AAPA fails to disclose a lens for forming an optical image of a subject.

YAMAMURA et al., on the other hand teaches a lens for forming an optical image of a subject.

More specifically, YAMAMURA et al. teaches a lens for forming an optical image of a subject (Page 1 lines 10 – 21 also paragraphs 0004 and 0007 – 0009).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of YAMAMURA et al. with the teachings of AAPA because in page 1 lines 5 – 8 and page 5 lines 4 – 17 also paragraphs 0009, 0012, 0013, and 0016 YAMAMURA et al. teaches that using the invention flaring problems can be reduced and corrected which in turn will produce an improved image.

Regarding **claim 9**, AAPA teaches a solid state image pick-up device formed on a chip, comprising: a pixel region; a first shift register for reading a signal charge from the pixel region (figure 8, item 205; Note: figures 7A,7B and 8 are prior art and the applicant has submitted an amendment to the drawing to label these figures as prior art); a second shift register having a lower driving frequency than that of the first shift register (figure 8, item 202 and paragraph 0014), wherein the first and second shift registers are arranged along

respectively different side portions of the chip (figure 8, items 205 and 202); an amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 8 item 207), outputting video signals (note this outputting of the video signal is not associated with any component as claimed so the examiner can consider any item such as item 207, 201, 204, 206 or any component as outputting video signal to be used later, in this case the examiner chooses item any one or a combination of these items).

However, AAPA fails to disclose a pad for supplying a voltage to the amplifier, the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged.

YAMAMURA et al., on the other hand teaches a pad for supplying a voltage to the amplifier, the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged.

More specifically, YAMAMURA et al. teaches a pad for supplying a voltage to the amplifier (pads supply all power to the pixel region), the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged (figures 1 – 2; pads arranged along vertical side of the chip away from the horizontal side when the horizontal registers are located).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of YAMAMURA et al. with the teachings of AAPA because in page 1 lines 5 – 8 and page 5 lines 4 – 17 also paragraphs 0009, 0012, 0013, and 0016 YAMAMURA et al. teaches that

using the invention flaring problems can be reduced and corrected which in turn will produce an improved image.

Regarding **claim 10**, AAPA teaches a solid state image pick-up device formed on a chip, comprising: a pixel region; a first shift register for reading a signal charge from the pixel region (figure 8, item 205; Note: figures 7A,7B and 8 are prior art and the applicant has submitted an amendment to the drawing to label these figures as prior art); a second shift register having a lower driving frequency than that of the first shift register (figure 8, item 202 and paragraph 0014), wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8, items 205 and 202); an amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 8 item 207), outputting video signals (note this outputting of the video signal is not associated with any component as claimed so the examiner can consider any item such as item 207, 201, 204, 206 or any component as outputting video signal to be used later, in this case the examiner chooses item any one or a combination of these items).

However, AAPA fails to disclose a pad for supplying a predetermined voltage or a ground voltage to an active element included in a pixel in the pixel region, the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged.

YAMAMURA et al., on the other hand teaches a pad for supplying a predetermined voltage or a ground voltage to an active element included in a

pixel in the pixel region, the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged.

More specifically, YAMAMURA et al. teaches a pad for supplying a predetermined voltage or a ground voltage to an active element included in a pixel in the pixel region (pads supply all power to the pixel region), the pad being arranged only along a side portion of the chip not parallel to the side portion along which the first shift register is arranged (figures 1 – 2; pads arranged along vertical side of the chip away from the horizontal side when the horizontal registers are located).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of YAMAMURA et al. with the teachings of AAPA because in page 1 lines 5 – 8 and page 5 lines 4 – 17 also paragraphs 0009, 0012, 0013, and 0016 YAMAMURA et al. teaches that using the invention flaring problems can be reduced and corrected which in turn will produce an improved image.

Regarding **claim 11**, as mentioned above in the discussion of claim 1, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other (figure 8 items 202 and 205).

Regarding **claim 12**, as mentioned above in the discussion of claim 9, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other (figure 8 items 202 and 205).

Regarding **claim 13**, as mentioned above in the discussion of claim 10, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other (figure 8 items 202 and 205).

Regarding **claim 14**, as mentioned above in the discussion of claim 1, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that the pad is arranged only along a side portion of the chip at an angle of 90 degrees to the side portion along which the first shift register is arranged (figure 8 items 202 and 205).

Regarding **claim 15**, as mentioned above in the discussion of claim 9, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that the pad is arranged only along a side portion of the chip at an angle of 90 degrees to the side portion along which the first shift register is arranged (figure 8 items 202 and 205).

Regarding **claim 16**, as mentioned above in the discussion of claim 10, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. Additionally, AAPA teaches that the pad is arranged only along a side portion of the chip at an angle of 90 degrees to the side portion along which the first shift register is arranged (figure 8 items 202 and 205).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (hereafter referred as AAPA; note the examiner is using the PgPub 2004/0057719 to refer to the paragraph numbers and such) in view of YAMAMURA et al. (US PgPub 2002/0025164) in further view of Itano et al. (US PgPub 2002/0051071).

Regarding **claim 3**, as mentioned above in the discussion of claim 2, AAPA in view of YAMAMURA et al. teaches all of the limitations of the parent claim. However, AAPA in view of YAMAMURA et al. fails to disclose that the active element comprises at least one selected from the group consisting of a transfer MOS transistor, a reset MOS transistor, a source follower input MOS transistor, and a selection MOS transistor. Itano et al., on the other hand teaches that the active element comprises at least one selected from the group consisting of a transfer MOS transistor, a reset MOS transistor, a source follower input MOS transistor, and a selection MOS transistor.

More specifically, Itano et al. teaches the active element comprises at least one selected from the group consisting of a transfer MOS transistor (figure

1 item 105, and paragraph 0006), a reset MOS transistor (figure 1 items 110a and 110b, and paragraph 0006), a source follower input MOS transistor (figure 1 item 107, and paragraphs 0006, 0048, 0051), and a selection MOS transistor (paragraph 0051).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Itano et al. with the teachings of AAPA in view of YAMAMURA et al. for reduction of size and in turn cost as taught in paragraph 0021 of Itano et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to USMAN KHAN whose telephone number is (571)270-1131. The examiner can normally be reached on Mon-Thru 6:45-4:15; Fri 6:45-3:15 or Alt. Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair>-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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4/30/2008
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